IN THE CLAIMS

1-12 (Cancelled)

13. (New) A method of manufacturing a semiconductor integrated circuit device including a memory cell constituted by a MISFET and a capacitor, comprising steps of:

forming the MISFET on a semiconductor substrate;

forming an insulating film on said MISFET;

depositing a first shielding film on said insulating film;

depositing, on an upper surface of said first shielding film,

a first conductive film, a capacitive insulating film comprised of a high-dielectric-constant material, and a second conductive film; patterning said second conductive film and said capacitive insulating film exclusive of said first shielding film; and thereby forming, on said first

shielding film, a capacitor constituted by a lower electrode comprised of said first conductive film, said capacitive insulating film, and an upper electrode comprised of said second conductive film; and

forming a second shielding film covering sidewalls of said upper electrode and said capacitor and being comprised of an insulating film contacting with an upper surface of said first shielding film,

wherein said capacitor is disposed on said MISFET through said insulating film,

said capacitor is covered with said first and second shielding films,

a plug is formed so that a conductive film is embedded into a first contact hole formed by removing said insulating film and said first shielding film on a source or drain region of said MISFET, said plug being connected to said lower electrode,

a second contact hole is formed in said insulating film disposed on the other of the source or drain region of said MISFET, and

the other of the source or drain region of said MISFET is connected through said second contact hole to a wiring formed on an upper portion of said insulating film.

14. (New) The method of manufacturing a semiconductor integrated circuit device according to claim 13,

wherein said first shielding film is formed so as to cover a forming region of said MISFET, and

said second contact hole is formed in said first shielding film.

15. (New) The method of manufacturing a semiconductor integrated circuit device according to claim 14,

wherein said second shielding film is formed so as to cover a formation region of said MISFET, and

said second contact hole is formed in said second shielding film.

16. (New) The method of manufacturing a semiconductor integrated circuit device according to claim 14,

wherein said first shielding film iscomprised of an insulating film.

17. (New) The method of manufacturing a semiconductor integrated circuit device according to claim 13,

wherein said step of forming the insulating film includes a step of annealing in a hydrogen atmosphere.

18. (New) A method of manufacturing a semiconductor integrated circuit device including a memory constituted by a MISFET and a capacitor, comprising steps of:

forming a MISFET on a semiconductor device;

forming an insulating film on said MISFET;

depositing a first shielding film on said insulating film;

depositing a first conductive film, a capacitive insulating film comprised of a ferroelectric material, and a second conductive film on said first shielding film;

patterning said second conductive film and said capacitive insulating film exclusive of said first shielding film; and thereby forming, on said first shielding film, a capacitor constituted by a lower electrode comprised of said first conductive film, said

capacitive insulating film, and an upper electrode comprised of the second conductive film; and

forming a second shielding film comprised of an insulating film so as to cover sidewalls of said upper electrode and said capacitor and contact with said first shielding film,

wherein said capacitor is disposed on said MISFET through said insulating film,

said capacitor is covered with said first and second shielding films,

said first shielding film is formed so as to cover a formation MISFET forming region,

a plug is formed so that a conductive film is embedded in a first contact hole formed by removing said insulating film and said first shielding film disposed on a source or drain region of said MISFET, said plug being connected to said lower electrode,

a second contact hole is formed in said insulating film disposed on the other of the source or drain region of said MISFET, and

the other of the source or drain region of said MISFET is connected to a wiring through said second contact hole.

19. (New) The method of manufacturing a semiconductor integrated circuit device according to claim 18,

wherein said second shielding film is formed so as to cover the said MISFET forming region,

said second contact hole is formed in said second shielding film, and

said first shielding film is comprised of an insulating film.

20. (New) The method of manufacturing a semiconductor integrated circuit device according to claim 18,

wherein said wiring is formed on an upper portion of said insulating film.